REMARKS

Applicant thanks Examiner for the detailed review of the application. Claims 1 and 3-20 remain pending.

Claim Objections

Claim 5 has been amended to remove the extraneous language left over from the previous amendment including the second period.

Claim Objections -35 USC § 112 first paragraph

The Office Action states:

> Claims 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant's claim 5 includes, "wherein the first message includes an InvalidateAllAndAcknowledge message, and wherein the shared cache, in response to receiving the write request referencing the block from the requesting processor core of the plurality of processor cores and the block not being owned, is to generate the InvalidateAllAndAcknowledge message, further in response to the block not being present in the shared cache and none of the plurality of processor cores being a custodian for the block," (currently amended claim 5). As a result, claim 1 includes a first message, which invalidates the block in the second processor core and acts as/provides a write acknowledge to the requesting core.

In claim 5, applicant further defines the first message as a InvalidateAndAcknowledge message, which still performs the invalidate of the second processor core, i.e. invalidate all cores except the requesting, and acts as an acknowledge to the requesting core. However, the generation

of the first message as an InvalidateAndAcknowledge, which in claim 1 is conditioned upon being "in response to receiving a write request…and the block not being owned," is further conditioned upon being "in response to the block not being present in the shared cache and none of the cores being a custodian for the block."

The Office Action points to paragraph 0020 of the application to indicate no support is provided for claim 5. However, applicant respectfully submits that adequate support is found at least in paragraph 0036 of the published application, which states the following:

> [0036] Next, if the state of X is present, not owned and no custodian, then in this instance, block X is present, but there is no custodian. This means that H does not know which cores have cached copies of X. Therefore, H sends a single INVALIDATEALLAND WRITEACKNOWLEDGE message around the ring. The INVALDIATE part is delivered to all cores, invalidating the cached copies. The WRITEACKNOWLEDGEMENT part is delivered only to core W, the processor that requested the write. H changes the custodian to W because no other core can now have a cached copy of X.

Note that paragraph 0036 is discussed as a response to discussion of a write flow from paragraph 0033, i.e. receiving a write request. Therefore, as can be seen, in response to a write request to block X and block X not being owned, not being present, and not having a custodian, as discussed immediately above in reference to the content of claim 5, then a single InvalidateAllAndAckknowledge message is sent around the ring. Part of the single message invalidates all cached copies of X, such as invalidating the block in the second processor core, and part of the single message is delivered to W (the core that requested the write) as a write acknowledgement, such as a write acknowledgement to the requesting core. Consequently, applicant respectfully submits that claim 5 has adequate support in applicant's disclosure.

Claim Rejections -35 USC § 103(a)

The Office Action states:

Claims 1, 3 – 6, 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Bordaz*** et al. (US Patent 6,195,728 B1), and in further view of ***Jennings*** (US Patent 6,134,631).

In regard to claims 1 and 18 - 20, Bordaz teaches:

"The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

Applicant's amended claim 1 includes, "a shared cache to be shared by the plurality of processor cores, wherein the shared cache includes logic, in response to receiving a write request referencing a block from a requesting processor core of the plurality of processor cores and the block not being owned, to generate a first message, and wherein the first message when received by a second processor core of the plurality of processor cores is to invalidate the block in the second processor core and the first message, when received by the requesting processor core, is also to act as a write acknowledgement to the requesting processor core." The Response to Arguments section of the Office Action states that applicant's previous response relying on claim 1 including a single message is beyond the scope of claim 1.

Applicant agrees that the specific term "a single message" is not recited in claim 1. However, note that the shared cache is to generate "the first message," which when received by the second processor core is to invalidate the block in the second processor core and the same first

message, when received by the requesting processor core, is also to act as a write acknowledge to the requesting core. Therefore, the use of a single message is only to convey that the same message, i.e. the first message, is to perform both the invalidation and the acknowledgment. As can be seen, this is a potential advantage for usage within a ring, i.e. transmission of the first message around the ring to both invalidate stale copies of a block as well as provide an appropriate acknowledgement to a requesting core without the antiquated numerous back and forth messages to both invalidate and acknowledge, which potentially reduces interconnect bandwidth performance.

With regard to the intended use remarks of The Office Action, applicant respectfully submits that claim 1 includes logic within the shared cache to generate the first message in response to receiving a write request and the block not being owned. Furthermore, after receipt of the same first message, the block is to be invalidated in the second core and the write request is acknowledged in the requesting core. Therefore, applicant respectfully submits that a reference would not merely have to disclose a capability of sending messages, but rather a reference that discloses logic with the specific capability of generating the first message in response to receiving the write request and the block being owned, as well as a second core capable of invalidating the block in response to receiving the first message and the requesting core capable of utilizing the first message as a write acknowledgment.

Therefore, applicant respectfully submits that neither Bordaz or Jennings convey or suggest a capability of the same first message to both invalidate in one core and acknowledge a requesting core, as described in applicant's claim 1. In fact the Office Action only cites at Page 7 the combination merely disclosing a capability of sending messages back forth, i.e. multiple messages, none of which include the capability of invalidating one core and acknowledging a requesting core.

Similar to the discussion above of intended use, applicant's claim 14 includes logic to perform the pertinent portions of the claims. Here, applicant's claim 14 includes, "wherein the

shared memory includes logic to generate an evict message referencing an address to an owning processor core of the plurality of cores in response to receiving a read request referencing the address from a requesting core of the plurality of cores and the owning processor core owning a block associated with the address." Applicant respectfully submits that neither Bordaz and Jenning disclose a capability of generating an evict message to an owning core for a block when a read request referencing the block is received from another core, but rather just the general capability of sending and receiving messages.

Applicant's claim 18 includes, "each of the plurality of blocks capable of being held in a not present state, a present and owned by a core of the plurality of cores state, a present, not owned, and a core of the plurality of cores is a custodian state, and a present, not owned, and no core of the plurality of cores is a custodian state." Similar to the discussion above, applicant's claim 18 includes logic to hold the block in the recited states. As a result, the logic is configured to indicate each of the blocks is held in one of the recited states. In contrast, neither Bordaz or Jennings disclose a capability of holding blocks in all of the recited states. The Office Action states that Bordaz discloses tag information to indicate if data is valid and if it is held exclusively. However, Bordaz does not disclose the capability of a block or cache line of being held in all of the four listed states in claim 18. Therefore, applicant respectfully submits that claim 18 includes a structural difference from the cited references, i.e. logic that is capable of indicating blocks are held in the four recited states, which is not disclosed as a capability in the references, where the logic is only capable of indicating if the data is value and if it is held exclusively.

Conclusion

Therefore, applicant respectfully request that independent claims 1, 14, and 18, as well as their currently pending dependent claims, are now in condition for allowance for at least the reasons stated above. If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, such as further discussion of the Intended Use argument section of The Office Action, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
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